950 to 1575 MHz Quadrature Modulator with Integrated Fractional-N PLL and VCO

Preliminary Technical Data

ADRF6750

FEATURES

IQ Modulator with Integrated Fractional-N PLL and VCO
Gain Control Span: 47dB in 1dB steps
Output frequency range: 950 MHz to 1575 MHz
Output Compression: +8.5 dBm
Output Intercept: +21 dBm
Noise Floor: -148 dBc/Hz
Baseband Modulation bandwidth: 250 MHz (1 dB)
Output Frequency Increment: 10 Hz
Functions with External VCO
SPI/I²C Serial Interface
Power Supply: +5 V/310 mA

DESCRIPTION

The ADRF6750 is a highly integrated quadrature modulator, frequency synthesizer, and programmable attenuator. The device covers an operating frequency range from 950MHz to 1575MHz and is primarily for use in satellite communication systems.

The ADRF6750 modulator includes a high modulus fractional-N frequency synthesizer with integrated VCO providing 10Hz frequency resolution, and a 47dB digitally controlled output attenuator with 1dB steps.

Control of all the on-chip registers is through a user selected SPI interface or I2C interface. The device operates from a single power supply ranging from 4.75V to 5.25V.

FUNCTIONAL BLOCK DIAGRAM

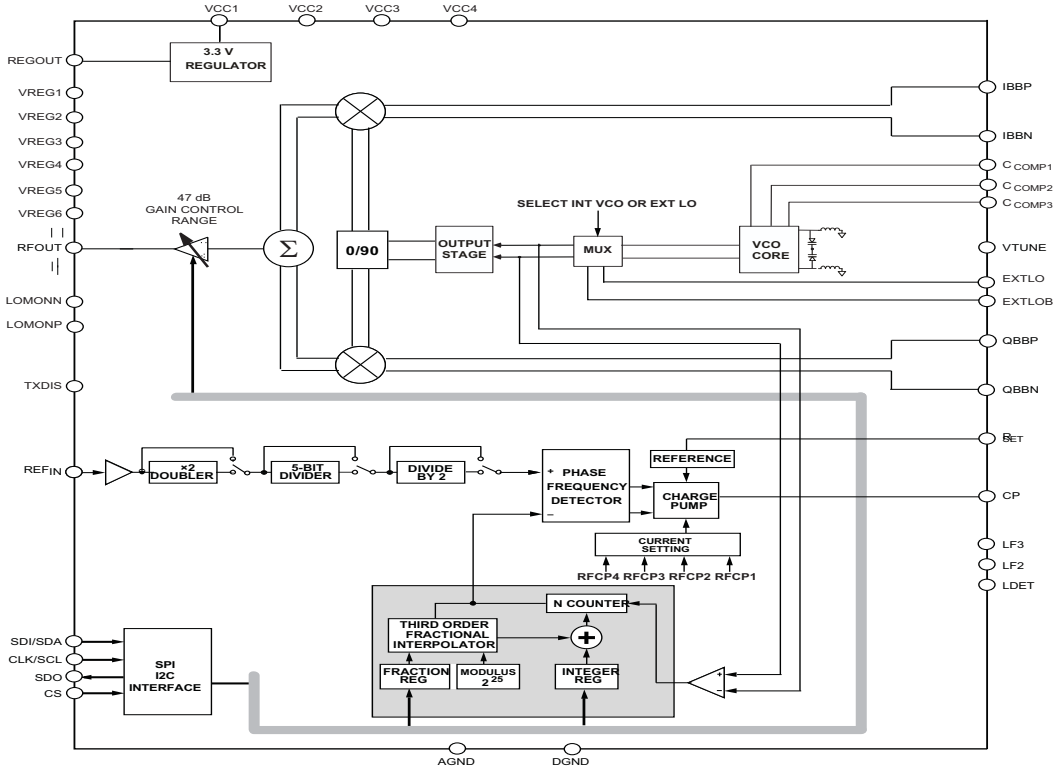

Figure 1.

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SPECIFICATIONS

Table 1. V_S = 5 V; Ambient Temperature (T_A) = 25°C; I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias; Minimum attenuation; Z_L=50Ω; Loop Bandwidth = 80 kHz; REFIN = 10 MHz PFD = 20MHz Baseband frequency = 1 MHz, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
RF OUTPUT	Pin RFOUT				
Operating Frequency Range		950		1575	MHz
Nominal Output Power			-2		dBm
Gain Flatness	Any 40 MHz		1		dB
Group Delay Flatness	Any 20 MHz		2		ns
Output P1dB			8.5		dBm
Output IP3	$F1_{BB}$ = 3.5 MHz, $F2_{BB}$ = 4.5 MHz, P_{OUT} = -6 dBm per tone		21		dBm
Output Return Loss	Minimum Attenuation, 50Ω reference impedance		-7		dB
LO Carrier Feedthrough	Pout = 0 dBm		-45		dBc
Vs. Gain	Pout = 0 dBm to -20 dBm		-40		dBc
	Pout = -20 dBm to -48 dBm		-60		dBm
2×LO Carrier Feedthrough			TBD		
Sideband Suppression			-45		dBc
Noise Floor	Pout = 0 dBm		-148		dBc/Hz
	Pout = 0 dBm to -20 dBm, Carrier Offset = 15 MHz		-143		dBc/Hz
	Pout = -20 dBm to -47 dBm, Carrier Offset = 15 MHz		-163		dBm/Hz
REFERENCE CHARACTERISTICS					
REFIN Input Frequency		10		20	MHz
REF_{IN} Input Sensitivity		0.4		VREG	V p-p
REF_{IN} Input Capacitance				10	pF
REF_{IN} Input Current				±100	µA
CHARGE PUMP					
I_{CP} Sink/Source	Programmable				
High Value	With R_{SET} = 4.7 kΩ		5		mA
Low Value			312.5		µA
Absolute Accuracy	With R_{SET} = 4.7 kΩ		2.5		%
VCO Gain	K_{VCO}		15		MHz/V
SYNTHESIZER SPECIFICATIONS	Loop bandwidth = 80 kHz				
Frequency Increment	FREF = 20 MHz		10		Hz
SPURS					
	Integer Boundary < Loop BW		-45		dBc
	> 10 MHz Offset from Carrier		-65		dBc
HARMONICS			-50		dBc
PHASE NOISE	Frequency = 950 to 1575 MHz[1]				
	@ 100 Hz offset, 20 MHz PFD frequency		–74		dBc/Hz
	@ 1kHz offset, 20 MHz PFD frequency		-81		dBc/Hz
	@ 10 kHz offset, 20 MHz PFD frequency		-89		dBc/Hz
	@ 100 kHz offset, 20 MHz PFD frequency		-104		dBc/Hz
	@ 1 MHz offset, 20 MHz PFD frequency		-115		dBc/Hz
	> 10 MHz offset , 20 MHz PFD frequency		-147		dBc/Hz
Integrated Phase Noise	1 KHz to 6 MHz integration bandwidth		0.7		°rms
Frequency Settling	Any step size, Max Frequency Error = 100 Hz		240		µs
Phase Detector Frequency				20	MHz
GAIN CONTROL					
Gain Range			47		dB
Step Size			1		dB
Relative Step Accuracy	Fixed Frequency, Adjacent Steps		±0.5		dB

Parameter	Conditions	Min	Typ	Max	Unit
	Vs. Frequency, 500 MHz, Adjacent Steps		±2		dB
Output Settling Time	Any step. Output power settled to = +/-0.2 dB		10		µs
OUTPUT DISABLE	Pin TXDIS				
Off Isolation	Gain = 0 dB to -20 dB, TXDIS High		-55		dBc
	Pout = -20 dB to -48 dB, TXDIS High		-75		dBm
Turn-On Settling Time	TXDIS High to Low (90% of envelope)		500		ns
Turn-Off Settling Time	TXDIS Low to High (10% of envelope)		500		ns
TXDIS High Level (Logic 1)		1.4			V
TXDIS Low Level (Logic 0)				0.6	V
MONITOR OUTPUT	Pins LOMONP, LOMONN				
Nominal Output Power			-24		dBm
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level			500		mV
Bandwidth (1 dB)			250		MHz
LOGIC INPUTS	SDI/SDA, CLK/SCL, CS				
V_{INH}, Input High Voltage		1.4			V
V_{INL}, Input Low Voltage				0.6	V
I_{INH}/I_{INL}, Input Current				±1	µA
C_{IN}, Input Capacitance				10	pF
LOGIC OUTPUTS	SDO				
V_{OH}, Output High Voltage		VREG– 0.4			V
I_{OH}				100	µA
V_{OL}, Output Low Voltage	I_{OL} = 500 µA			0.4	V
I^2C INTERFACE TIMING	(see Figure 5)				
SCL Clock Frequency				400	kHz
SCL Pulse Width High	t_{HIGH}	600			ns
SCL Pulse Width Low	t_{LOW}	1300			ns
Start Condition Hold Time	$t_{HD;STA}$	600			ns
Start Condition Setup Time	$t_{SU;STA}$	600			ns
Data Setup Time	$t_{SU;DAT}$	100			ns
Data Hold Time	$t_{HD;DAT}$	300			ns
Stop Condition Setup Time	$t_{SU;STO}$	600			ns
Data Valid Time	$t_{VD;DAT}$			900	ns
Data Valid Acknowledge Time	$t_{VD;ACK}$			900	ns
Bus Free Time	t_{BUF}	1300			ns
SPI INTERFACE TIMING	(see Figure 9)				
f_{SCLK}				20	MHz
CLK high pulse width	t_1	15			ns
CLK low pulse width	t_2	15			ns
Hold time (Start Condition)	t_3	5			ns
Data setup time	t_4	10			ns
Data hold time	t_5	5			ns
Setup time (Stop Condition)	t_6	5			ns
SDO Access Time	t_7	15			ns
CS to SDO High Impedance	t_8			25	ns
POWER SUPPLIES	Pins VCC1, VCC2, VCC3, VCC4, VREG1, VREG2, VREG3, VREG4, REGVOUT				
	REGVOUT normally connected to VREG1, VREG2, VREG3, VREG4				
Voltage Range	VCC1, VCC2, VCC3, VCC4	4.75	5	5.25	V
	VREG1, VREG2, VREG3, VREG4		3.3		V
	REGVOUT		3.3		V

Parameter	Conditions	Min	Typ	Max	Unit
Supply Current	VCC1, VCC2, VCC3 and VCC3 combined (REGVOUT connected to VREG1, VREG2, VREG3, VREG4)		310		mA
Operating Temperature		0		70	°C

ABSOLUTE MAXIMUM RATINGS

Table 2. S-MOD Absolute Maximum Ratings

Parameter	Rating
Supply Voltage VCC1, VCC2, VCC3, VCC4	-0.3 to 6 V
Supply Voltage VREG1, VREG2, VREG3, VREG4	-0.3 to 4 V
IBBP, IBBN, QBBP, QBBN	0 to 2.5 V
Digital I/O	-0.3 to 4 V
REFIN, CP, RSET, CCOMP1, CCOMP2	-0.3 to 4 V
θ_{JA} (Exposed Paddle Soldered Down)	26 °C/W
Maximum Junction Temperature	120°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

Table 3. Pin Function Descriptions

Pin Nr.	Mnemonic	Description
11	VCC1	**3.3 V Regulator Power Supply:** A 5 V power supply should be applied to VCC1 which should be decoupled with power supply decouplng capacitors. VCC2, VCC3 and VCC4 should be connected to the same 5 V power supply.
55, 56 41, 42 1	VCC2 VCC3 VCC4	**Positive Power Supplies for IQ Modulator:** Connect to the same 5 V power supply as VCC1. Each VCC pin should have separate power supply decoupling.
12	REGOUT	**3.3 V Regulator Output:** REGVOUT provides a 3.3 V output supply which drives VREG1, VREG2, VREG3, VREG4, VREG5 and VREG6.
13 14 15 16 31 36	VREG1 VREG2 VREG3 VREG4 VREG5 VREG6	**Positive Power Supplies for PLL Synthesizer, VCO and Serial Port:** These pins should be connected to REGVOUT (3.3 V) and should be separately decoupled.
6,19, 20, 21, 24, 37, 39, 40, 46, 47, 49, 50, 51, 52, 53, 54	AGND	**Analog Ground:** Connect to a low-impedance ground plane
32	DGND	**Digital Ground:** Connect to the same low-impedance ground plane as the AGND pins
2 3 4 5	IBBP IBBN QBBN QBBP	**Differential In-Phase and Quadrature Baseband Inputs:** These high impedance inputs must be dc-biased to approximately 500 mV dc, and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. This results in a differential drive of 0.9 V p-p with a 500 mV dc bias, resulting in a single sideband output power of approximately 0 dBm. These inputs are not self-biased and must be externally biased.
33	CCOMP1	**Internal Compensation Node:** This pin must be decoupled to ground with a 100 nF capacitor.
34	CCOMP2	**Internal Compensation Node:** This pin must be decoupled to ground with a 100 nF capacitor.
35	CCOMP3	**Internal Compensation Node:** This pin must be decoupled to ground with a 100 nF capacitor
38	VTUNE	**Control Input to the VCO:** This voltage determines the output frequency and is derived from filtering the CP output voltage.
7	RSET	**Charge Pump Current Set:** Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{23.5}{R_{SET}}$$ where: R_{SET} = 4.7 kΩ. $I_{CP\,max}$ = 5 mA.
9	CP	**Charge Pump Output:** When enabled, this provides ±I_{CP} to the external loop filter, which in turn, drives the internal VCO.
27	CS	**Chip Select:** CMOS Input. When CS is high, the data stored in the shift registers is loaded into one of thirty latches. In I²C mode when CS is high, the slave address of the device is 60H and when low, the slave address is 40H.
29	SDI/SDA	**Serial Data Input for SPI/I²C Port:** This input is a high impedance CMOS data input. Data is loaded in an 8-bit word in SPI mode.
30	CLK/SCL	**Serial Clock Input for SPI/I²C Port:** This serial clock is used to clock in the serial data to the registers. This input is a high impedance CMOS input.
28	SDO	**Serial Data Output for SPI Port:** Register states can be read back on the SDO data output line.
17	REFIN	**Reference Input:** This is a high impedance CMOS input which should be ac-coupled.
18	REFINB	**Reference Input B:** This should be either be grounded or ac-coupled to ground.
48	RFOUT	**RF Output:** Single-ended, 50 Ω internally biased RF output. Pin must be ac-coupled to the load. Nominal ouptut power is 0 dBm for a single sideband baseband drive of 0.9 V pp differential on the I and Q inputs (Attenuation = Min)
45	TXDIS	**Output Disable:** This pin can be used to disable the RF output. Connect to high logic level to disable output. Connect to low logic level for normal operation.

25 26	LOMONP LOMONN	**Differential Monitor Output:** Provides a replica of the internal local oscillator frequency (1XLO) at approximatley -24 dBm. Open collector outputs, terminate with external resistors to VCC. This output can be disabled through serial port programming. These should be grounded if not used.
22 23	EXTLO EXTLOB	**Differential External LO Inputs:** These inputs are used to drive the 2xLO signal to the modulator directly without using the on-chip VCO or PLL synthesizer possibly. There are two modes which are useful. 1. Close the PLL using an external VCO and the on-chip PLL synthesizer. In this case, the charge pump output is connected to the external loop filter which drives an external VCO. The output of the external VCO can be connected to the EXTLO input while EXTLOB is decoupled to gnd using a 100pF capacitor or alternatively the output of the external VCO can drive a BALUN the outputs of which drive both EXTLO and EXTLOB inputs. Vtune is not connected. Note the external VCO needs to operate at a frequency of 2xLO. Also the internal VCO needs to be powered down by setting CR28[5] = '1'. CR27[3] needs to be set to '1' to mux the external VCO signal through to the modulator. Both EXTLO and EXTLOB need to be biased to 3.3V. 2. Use an external 2xLO to generate the 2xLO signal to the modulator bypassing the on-chip PLL. In this case the on-chip PLL needs to be powered down by setting CR12[2] = '1'. CR27[3] needs to be set to '1' to mux the external 2xLO signal through to the modulator. Both EXTLO and EXTLOB need to be biased to 3.3V. Again a BALUN can be used to drive the EXTLO inputs differentially or EXTLO can be driven single-ended with EXTLOB decoupled to gnd using a 100pF capacitor.
10 8	LF2 LF3	**Extra Loop Filter Pins for Fastlock:** Pins are used to reduce lock time. These should be left O/C if not used. Contact Analog Devices for more details.
44	LDET	**Lock Detect:** This pin indicates the state of the PLL, a high level indicates a locked condition while a low level indicates a loss of lock condition.
43	MUXOUT	**Muxout:** This output is a test output for diagnostic use only. It should be left O/C by the customer.
PADDLE	EP	**Exposed Paddle:** Connect to ground plane via a low impedance path

I²C INTERFACE TIMING

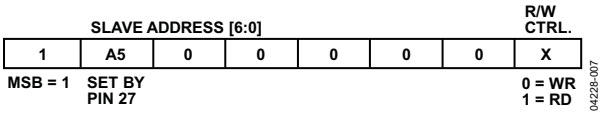

Figure 1. Slave Address Configuration

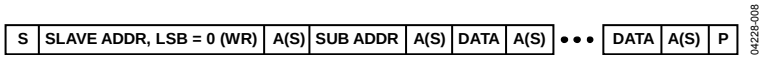

Figure 2. I²C Write Data Transfer

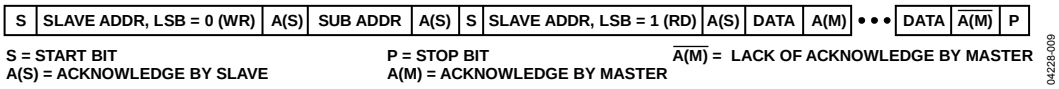

Figure 3. I²C Read Data Transfer

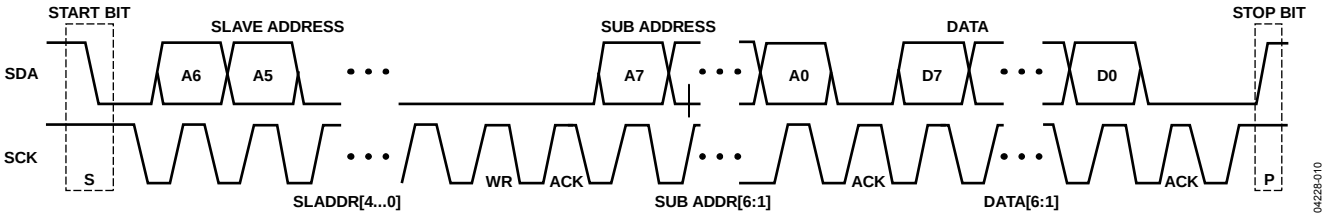

Figure 4. I²C Data Transfer Timing

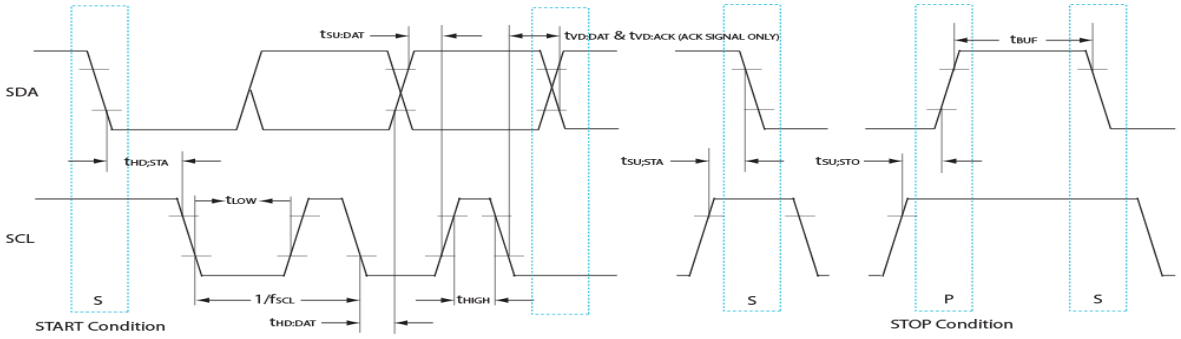

Figure 5. I²C Port Timing Diagram

SPI INTERFACE TIMING

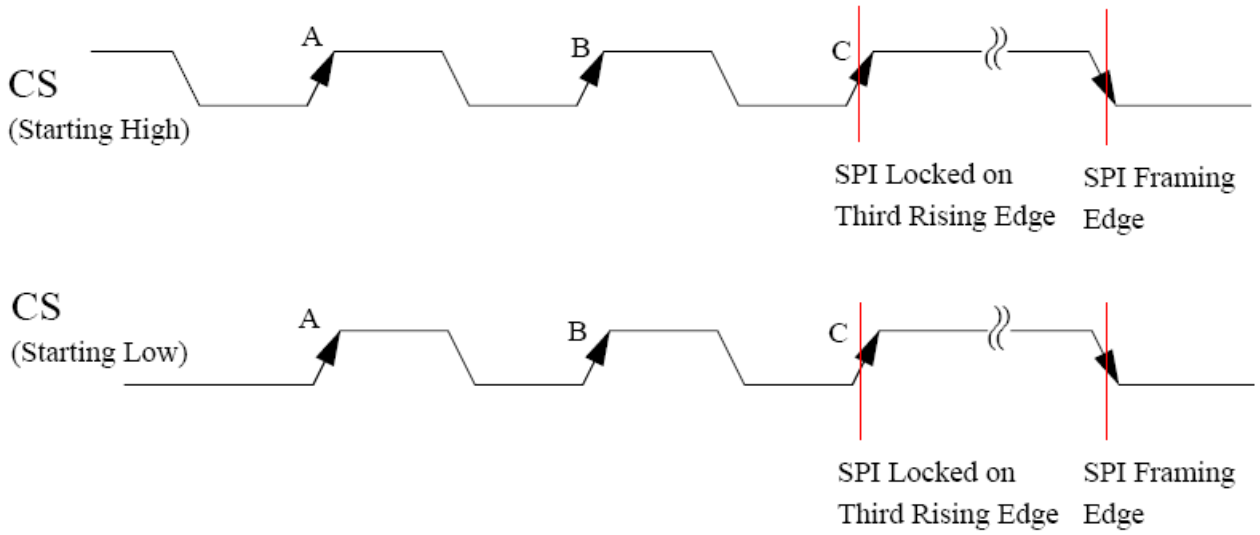

Figure 6. Selecting the SPI Protocol

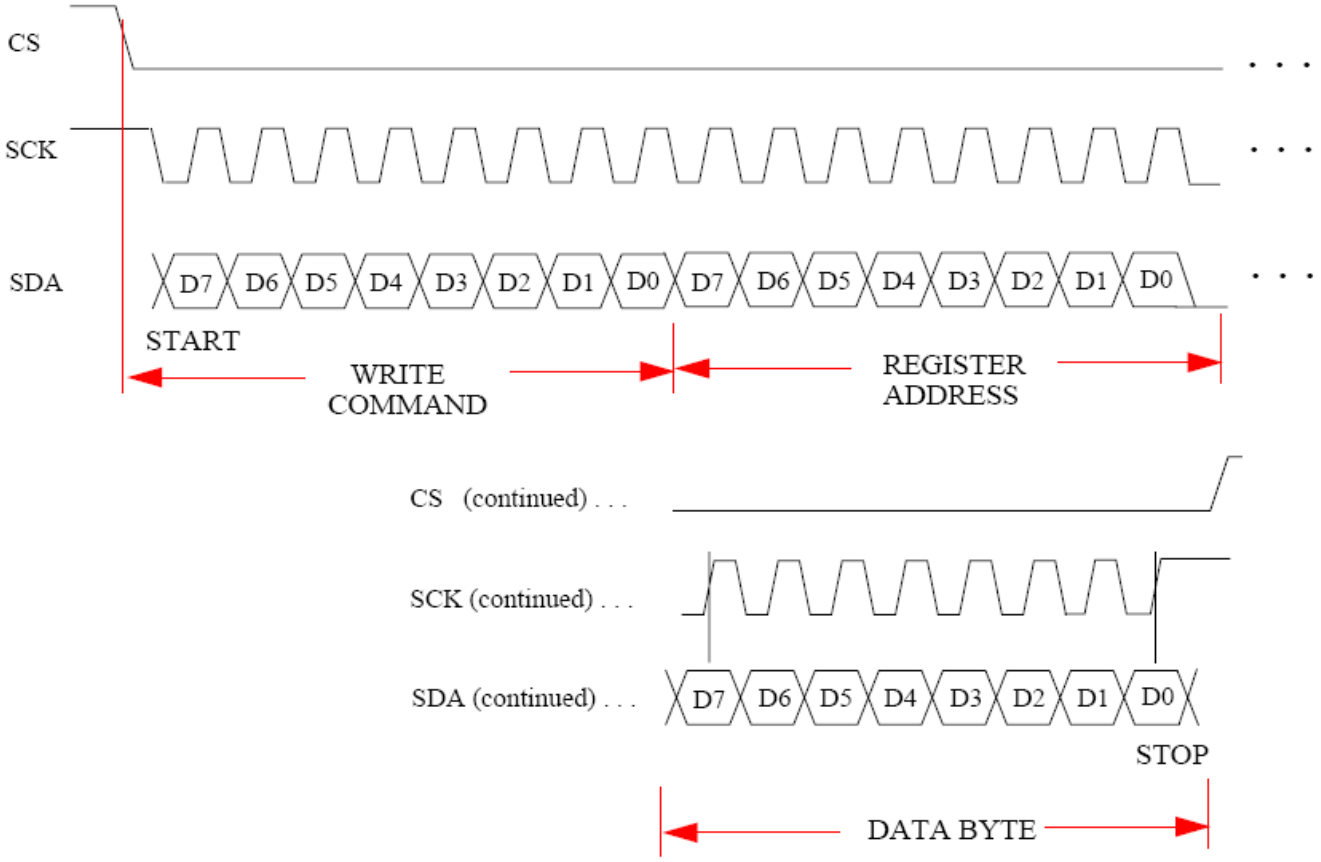

Figure 7. SPI Byte Write Example

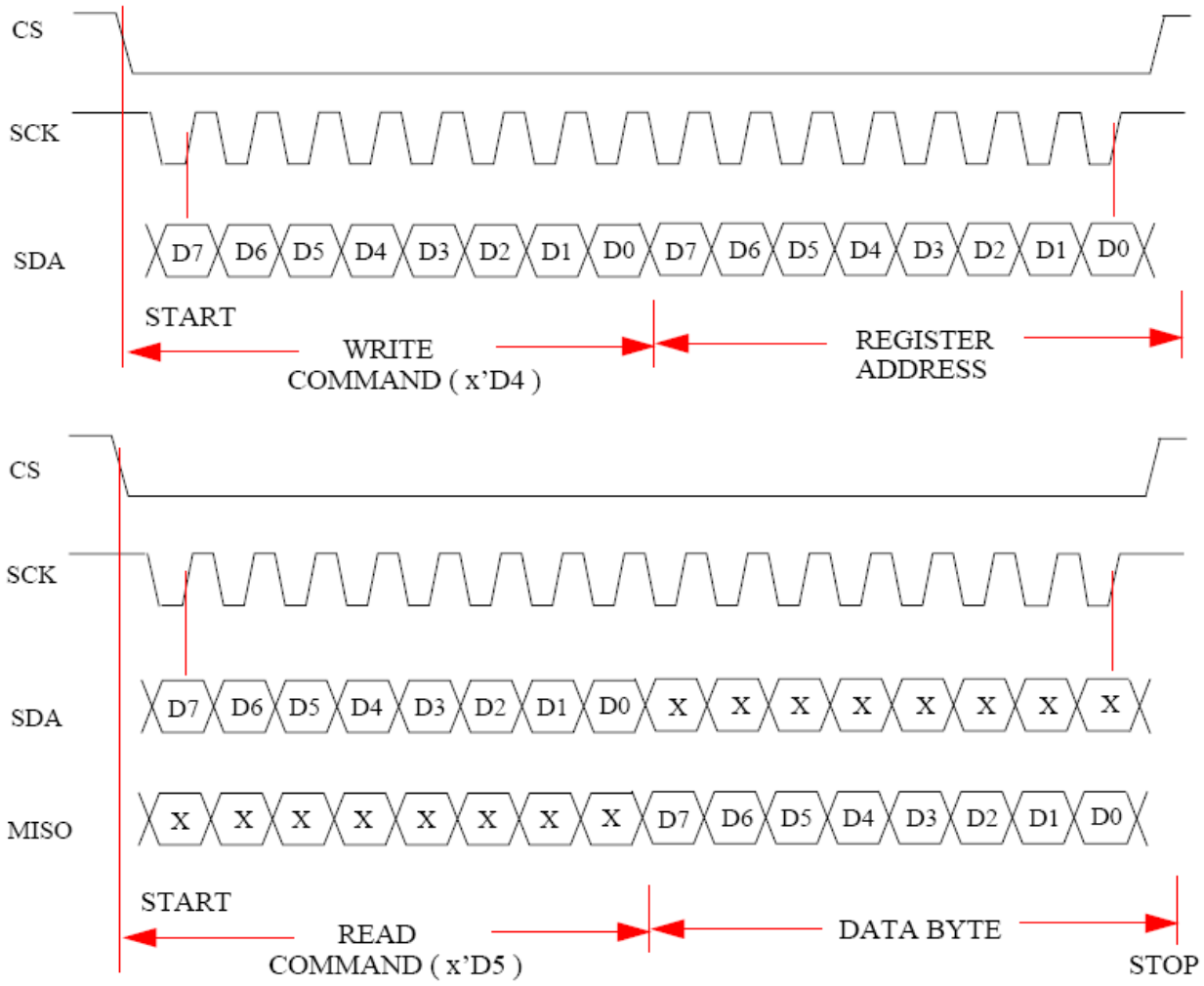

Figure 8. SPI Byte Read Example

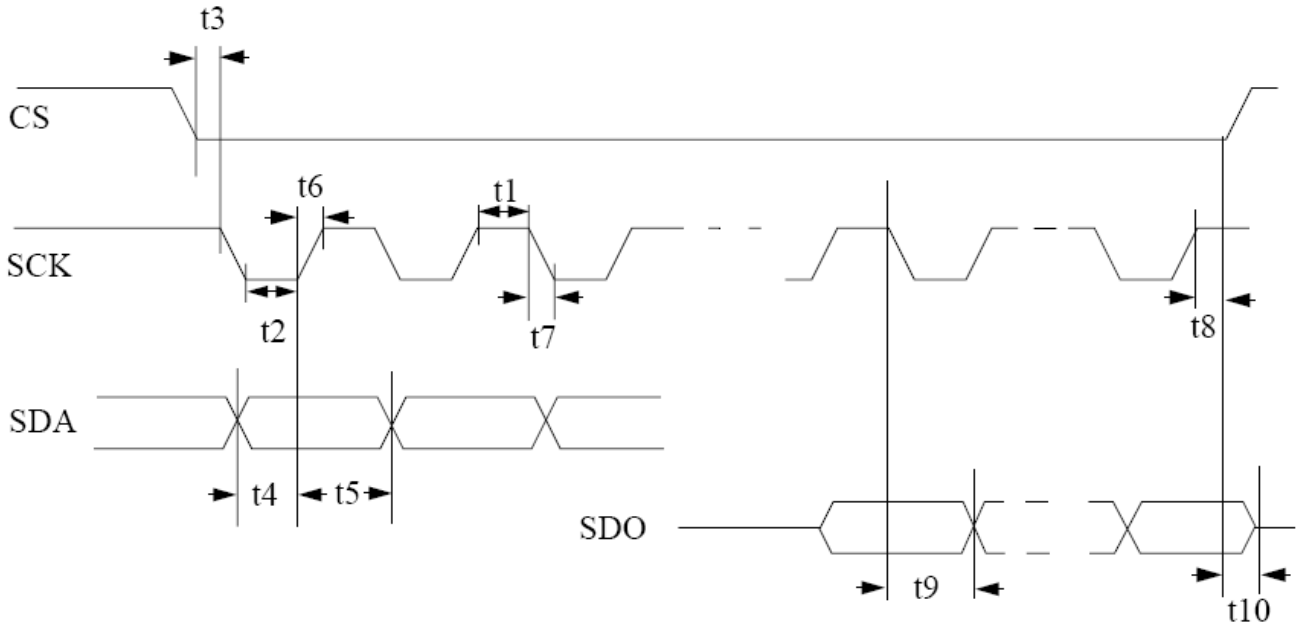

Figure 9. SPI Port Timing Diagram

REGISTER MAP.

Table 4. CR33 – Revision Register

CR33 – Addr = 21h	Revision Register
Bit	Function
CR33[7]	Revision Code
CR33[6]	Revision Code
CR33[5]	Revision Code
CR33[4]	Revision Code
CR33[3]	Revision Code
CR33[2]	Revision Code
CR33[1]	Revision Code
CR33[0]	Revision Code

Table 5. CR32 – Reserved Register

CR32 – Addr = 20h	Reserved Register
Bit	Function
CR32[7]	Reserved
CR32[6]	Reserved
CR32[5]	Reserved
CR32[4]	Reserved
CR32[3]	Reserved
CR32[2]	Reserved
CR32[1]	Reserved
CR32[0]	Reserved

Table 6. CR31 – Reserved Register

CR31 – Addr = 1Fh	Reserved Register
Bit	Function
CR31[7]	Reserved
CR31[6]	Reserved
CR31[5]	Reserved
CR31[4]	Reserved
CR31[3]	Reserved
CR31[2]	Reserved
CR31[1]	Reserved
CR31[0]	Reserved

Table 7. CR30 – Attenuator Register

CR30 – Addr = 1Eh	Attenuator Register
Bit	Function
CR30[7]	Reserved. Set to '0'
CR30[6]	Reserved. Set to '0'
CR30[5:0]	Attenuator A5:A0 000000: 0dB 000001: 1dB 000010: 2dB …….. 101101: 45dB 101110: 46dB 101111: 47dB

Table 8. CR29 – Modulator Register

CR29 – Addr = 1Dh	Modulator
Bit	Function
CR29[7]	Reserved. Set to '0'
CR29[6]	Reserved. Set to '0'
CR29[5]	Reserved. Set to '0'
CR29[4]	Reserved. Set to '0'
CR29[3]	Reserved. Set to '0'
CR29[2]	Reserved. Set to '0'
CR29[1]	Reserved. Set to '0'
CR29[0]	Power Up Modulator: 0: Power Down (D) 1: Power Up

Table 9. CR28 – Reserved Register

CR28 – Addr = 1Ch	Reserved
Bit	Function
CR28[7]	Reserved. Set to '0'
CR28[6]	Synth Power Down: 0: Power Up (D) 1: Power Down
CR28[5]	VCO Power Down: 0: Power Up (D) 1: Power Down
CR28[4]	Reserved. Set to '0'
CR28[3]	Reserved. Set to '0'
CR28[2]	Reserved. Set to '0'
CR28[1]	Reserved. Set to '0'
CR28[0]	Reserved. Set to '1'

Table 10. CR27 – RF Monitor Output Register

CR27 – Addr = 1Bh	Reserved
Bit	Function
CR27[7]	Reserved. Set to '0'
CR27[6]	Reserved. Set to '0'
CR27[5]	Reserved. Set to '0'
CR27[4]	Reserved. Set to '0'
CR27[3]	Modulator LO Control: 0: Internal VCO -> Modulator 1: External LO -> Modulator
CR27[2]	Power Up Monitor Output: 0: Power Down (D) 1: Power Up
CR27[1:0]	Monitor Output Power into 50Ω: 00: -24dBm (D) 01: -18dBm 10: -12dBm 11: -6dBm

Table 11. CR26 – Reserved Register

CR26 – Addr = 1Ah	Reserved
Bit	Function
CR26[7]	Reserved. Set to '0'
CR26[6]	Reserved. Set to '0'
CR26[5]	Reserved. Set to '0'
CR26[4]	Reserved. Set to '0'
CR26[3]	Reserved. Set to '0'
CR26[2]	Reserved. Set to '0'
CR26[1]	Reserved. Set to '0'
CR26[0]	Reserved. Set to '0'

Table 12. CR25 – Reserved Register

CR25 – Addr = 19h	Reserved
Bit	Function
CR25[7]	Reserved. Set to '0'
CR25[6]	Reserved. Set to '0'
CR25[5]	Reserved. Set to '1'
CR25[4]	Reserved. Set to '1'
CR25[3]	Reserved. Set to '0'
CR25[2]	Reserved. Set to '0'
CR25[1]	Reserved. Set to '1'
CR25[0]	Reserved. Set to '0'

Table 13. CR24 Reserved Register

CR24 – Addr = 18h	Autocal
Bit	Function
CR24[7]	Reserved. Set to '0'
CR24[6]	Reserved. Set to '0'
CR24[5]	Reserved. Set to '0'
CR24[4]	Reserved. Set to '1'
CR24[3]	Reserved. Set to '1'
CR24[2]	Reserved. Set to '0'
CR24[1]	Reserved. Set to '0'
CR24[0]	Reserved. Set to '0'

Table 14. CR23 – Lock Detector Control Register

CR23 – Addr = 17h	Lock Detector Control
Bit	Function
CR23[7]	Reserved. Set to '0'
CR23[6]	Reserved. Set to '1'
CR23[5]	Reserved. Set to '1'
CR23[4]	Lock Detector Enable: 0: LD Disabled (D) 1: LD Enabled
CR23[3]	Reserved. Set to '0'
CR23[2]	Reserved. Set to '1'
CR23[1]	Reserved. Set to '0'
CR23[0]	Reserved. Set to '0'

Table 15. CR22 – Reserved Register

CR22 – Addr = 16h	Reserved
Bit	Function
CR22[7]	Reserved. Set to '0'
CR22[6]	Reserved. Set to '0'
CR22[5]	Reserved. Set to '0'
CR22[4]	Reserved. Set to '0'
CR22[3]	Reserved. Set to '0'
CR22[2]	Reserved. Set to '0'
CR22[1]	Reserved. Set to '0'
CR22[0]	Reserved. Set to '0'

Table 16. CR21 – Reserved Register

CR21 – Addr = 15h	**Reserved**
Bit	Function
CR21[7]	Reserved. Set to '0'
CR21[6]	Reserved. Set to '0'
CR21[5]	Reserved. Set to '0'
CR21[4]	Reserved. Set to '0'
CR21[3]	Reserved. Set to '0'
CR21[2]	Reserved. Set to '0'
CR21[1]	Reserved. Set to '0'
CR21[0]	Reserved. Set to '0'

Table 17. CR20 – Reserved Register

CR20 – Addr = 14h	**Reserved**
Bit	Function
CR20[7]	Reserved. Set to '0'
CR20[6]	Reserved. Set to '0'
CR20[5]	Reserved. Set to '0'
CR20[4]	Reserved. Set to '0'
CR20[3]	Reserved. Set to '0'
CR20[2]	Reserved. Set to '0'
CR20[1]	Reserved. Set to '0'
CR20[0]	Reserved. Set to '0'

Table 18. CR19 – Reserved Register

CR19 – Addr = 13h	**Reserved**
Bit	Function
CR19[7]	Reserved. Set to '0'
CR19[6]	Reserved. Set to '0'
CR19[5]	Reserved. Set to '0'
CR19[4]	Reserved. Set to '0'
CR19[3]	Reserved. Set to '0'
CR19[2]	Reserved. Set to '0'
CR19[1]	Reserved. Set to '0'
CR19[0]	Reserved. Set to '0'

Table 19. CR18 – Reserved Register

CR18 – Addr = 12h	**Reserved**
Bit	Function
CR18[7]	Reserved. Set to '0'
CR18[6]	Reserved. Set to '0'
CR18[5]	Reserved. Set to '0'
CR18[4]	Reserved. Set to '0'
CR18[3]	Reserved. Set to '0'
CR18[2]	Reserved. Set to '0'
CR18[1]	Reserved. Set to '0'
CR18[0]	Reserved. Set to '0'

Table 20. CR17 – Reserved Register

CR17 – Addr = 11h	**Reserved**
Bit	Function
CR17[7]	Reserved. Set to '0'
CR17[6]	Reserved. Set to '0'
CR17[5]	Reserved. Set to '0'
CR17[4]	Reserved. Set to '0'
CR17[3]	Reserved. Set to '0'
CR17[2]	Reserved. Set to '0'
CR17[1]	Reserved. Set to '0'
CR17[0]	Reserved. Set to '0'

Table 21. CR16 – Reserved Register

CR16 – Addr = 10h	**Reserved**
Bit	Function
CR16[7]	Reserved. Set to '0'
CR16[6]	Reserved. Set to '0'
CR16[5]	Reserved. Set to '0'
CR16[4]	Reserved. Set to '0'
CR16[3]	Reserved. Set to '0'
CR16[2]	Reserved. Set to '0'
CR16[1]	Reserved. Set to '0'
CR16[0]	Reserved. Set to '0'

Table 22. CR15 – Reserved Register

CR15 – Addr = 0Fh	**Reserved**
Bit	Function
CR15[7]	Reserved. Set to '0'
CR15[6]	Reserved. Set to '0'
CR15[5]	Reserved. Set to '0'
CR15[4]	Reserved. Set to '0'
CR15[3]	Reserved. Set to '0'
CR15[2]	Reserved. Set to '0'
CR15[1]	Reserved. Set to '0'
CR15[0]	Reserved. Set to '0'

Table 23. CR14 – TxDis Control Register

CR14 – Addr = 0Eh	**Reserved**
Bit	Function
CR14[7]	Reserved. Set to '0'
CR14[6]	Reserved. Set to '0'
CR14[5]	TxDis_Attenuator: 0: Atten always Enabled (D) 1: Disable Atten when TxDis =1
CR14[4]	TxDis_LOBuf: 0: LOBuf always Enabled (D) 1: Disable LOBuf when TxDis =1
CR14[3]	TxDis_QuadDiv: 0: QuadDiv always Enabled (D) 1: Disable QuadDiv when TxDis =1
CR14[2]	Reserved. Set to '0'
CR14[1]	TxDis_LOX2: 0: LOX2 always Enabled (D) 1: Disable LOX2 when TxDis =1
CR14[0]	TxDis_RFMON: 0: RFMON always Enabled (D) 1: Disable RFMON when TxDis =1

Table 24. CR13 – Reserved Control Register

CR13 – Addr = 0Dh	**Reserved**
Bit	Function
CR13[7]	Reserved. Set to '0'
CR13[6]	Reserved. Set to '0'
CR13[5]	Reserved. Set to '0'
CR13[4]	Reserved. Set to '1'
CR13[3]	Reserved. Set to '1'
CR13[2]	Reserved. Set to '0'
CR13[1]	Reserved. Set to '0'
CR13[0]	Reserved. Set to '0'

Table 25. CR12 – Power Up Register

CR12 – Addr = 0Ch	**Reserved**
Bit	Function
CR12[7]	Reserved. Set to '0'
CR12[6]	Reserved. Set to '0'
CR12[5]	Reserved. Set to '0'
CR12[4]	Reserved. Set to '0'
CR12[3]	Reserved. Set to '1'
CR12[2]	Power Down: 0: Power Up PLL (D) 1: Power Down PLL
CR12[1]	Reserved. Set to '0'
CR12[0]	Reserved. Set to '0'

Table 26. CR11 – Reserved Register

CR11 – Addr = 0Bh	**Reserved**
Bit	Function
CR11[7]	Reserved. Set to '0'
CR11[6]	Reserved. Set to '0'
CR11[5]	Reserved. Set to '0'
CR11[4]	Reserved. Set to '0'
CR11[3]	Reserved. Set to '0'
CR11[2]	Reserved. Set to '0'
CR11[1]	Reserved. Set to '0'
CR11[0]	Reserved. Set to '0'

Table 27. CR10 – Reference Frequency Control Register

CR10 – Addr = 0Ah	**Reserved**
Bit	Function
CR10[7]	Reserved. Set to '0' [DB]:
CR10[6]	R/2 Divider Enable [DB]: 0: Bypass R/2 Divider 1: Enable R/2 Divider
CR10[5]	R Doubler Enable [DB]: 0: Disable Doubler (D) 1: Enable Doubler
CR10[4:0]	5-Bit R Divider Setting [DB]: 00001: Divide by 1 00010: Divide by 2 ……... 11111: Divide by 31 00000: Divide by 32 (D)

Table 28. CR9 – Charge Pump Current Setting Register

CR9 – Addr = 09h	Charge Pump Current Setting
Bit	Function
CR9[7:4]	Charge Pump Current (Rset = 4k7) [DB]: 0000: 0.31mA (D) 0001: 0.63mA 0010: 0.94mA 0011: 1.25mA 0100: 1.57mA 0101: 1.88mA 0110: 2.19mA 0111: 2.50mA 1000: 2.81mA 1001: 3.13mA 1010: 3.44mA 1011: 3.75mA 1100: 4.06mA 1101: 4.38mA 1110: 4.69mA 1111: 5.00mA
CR9[3]	Reserved. Set to '0'
CR9[2]	Reserved. Set to '0'
CR9[1]	Reserved. Set to '0'
CR9[0]	Reserved. Set to '0'

Table 29. CR8 – Reserved Register

CR8 – Addr = 08h	Reserved
Bit	Function
CR8[7]	Reserved. Set to '0'
CR8[6]	Reserved. Set to '0'
CR8[5]	Reserved. Set to '0'
CR8[4]	Reserved. Set to '0'
CR8[3]	Reserved. Set to '0'
CR8[2]	Reserved. Set to '0'
CR8[1]	Reserved. Set to '0'
CR8[0]	Reserved. Set to '0'

Table 30. CR7 – Integer Word Setting (MSB) Register

CR7 – Addr = 07h	Integer Word Setting (MSB)
Bit	Function
CR7[7]	Reserved. Set to '0'
CR7[6]	Reserved. Set to '0'
CR7[5]	Reserved. Set to '0'
CR7[4]	Reserved. Set to '0'
CR7[3]	Integer Word N11 [DB]
CR7[2]	Integer Word N10 [DB]
CR7[1]	Integer Word N9 [DB]
CR7[0]	Integer Word N8 [DB]

Table 31. CR6 – Integer Word Setting (LSB) Register

CR6 – Addr = 06h	Integer Word Setting (MSB)
Bit	Function
CR6[7]	Integer Word N7 [DB]
CR6[6]	Integer Word N6 [DB]
CR6[5]	Integer Word N5 [DB]
CR6[4]	Integer Word N4 [DB]
CR6[3]	Integer Word N3 [DB]
CR6[2]	Integer Word N2 [DB]
CR6[1]	Integer Word 1 [DB]
CR6[0]	Integer Word 0 [DB]

Table 32. CR5 – Reference Divider Enable Register

CR5 – Addr = 05h	Reference Divider Enable
Bit	Function
CR5[7]	Reserved. Set to '0'
CR5[6]	Reserved. Set to '0'
CR5[5]	Reserved. Set to '0'
CR5[4]	5-Bit R Divider Enable [DB]: 0: Disable 5-Bit R Divider (D) 1: Enable 5-Bit R Divider
CR5[3]	Reserved. Set to '0'
CR5[2]	Reserved. Set to '0'
CR5[1]	Reserved. Set to '0'
CR5[0]	Reserved. Set to '0'

Table 33. CR4 – Reserved Register

CR4 – Addr = 04h	Reserved
Bit	Function
CR4[7]	Reserved. Set to '0'
CR4[6]	Reserved. Set to '0'
CR4[5]	Reserved. Set to '0'
CR4[4]	Reserved. Set to '0'
CR4[3]	Reserved. Set to '0'
CR4[2]	Reserved. Set to '0'
CR4[1]	Reserved. Set to '0'
CR4[0]	Reserved. Set to '1' (D)

Table 34. CR3 – Fractional Word 1 Register

CR3 – Addr = 03h	Fractional Word 1
Bit	Function
CR3[7]	Reserved. Set to '0'
CR3[6]	Reserved. Set to '0'
CR3[5]	Reserved. Set to '0'
CR3[4]	Reserved. Set to '0'
CR3[3]	Reserved. Set to '0'
CR3[2]	Reserved. Set to '0'
CR3[1]	Reserved. Set to '0'
CR3[0]	Fraction Word F24 - MSB [DB]

Table 35. CR2 – Fractional Word 2 Register

CR2 – Addr = 02h	Fractional Word 2
Bit	Function
CR2[7]	Fraction Word F23 [DB]
CR2[6]	Fraction Word F22 [DB]
CR2[5]	Fraction Word F21 [DB]
CR2[4]	Fraction Word F20 [DB]
CR2[3]	Fraction Word F19 [DB]
CR2[2]	Fraction Word F18 [DB]
CR2[1]	Fraction Word F17 [DB]
CR2[0]	Fraction Word F16 [DB]

NOTE: DB = Double Buffered. Load on CR0 write.

Table 36. CR1 – Fractional Word 3 Register

CR1 – Addr = 01h	Fractional Word 3
Bit	Function
CR1[7]	Fraction Word F15 [DB]
CR1[6]	Fraction Word F14 [DB]
CR1[5]	Fraction Word F13 [DB]
CR1[4]	Fraction Word F12 [DB]
CR1[3]	Fraction Word F11 [DB]
CR1[2]	Fraction Word F10 [DB]
CR1[1]	Fraction Word F9 [DB]
CR1[0]	Fraction Word F8 [DB]

Table 37. CR0 – Fractional Word 4 Register

CR0 – Addr = 00h	Fractional Word 3
Bit	Function
CR0[7]	Fraction Word F7 [DB]
CR0[6]	Fraction Word F6 [DB]
CR0[5]	Fraction Word F5 [DB]
CR0[4]	Fraction Word F4 [DB]
CR0[3]	Fraction Word F3 [DB]
CR0[2]	Fraction Word F2 [DB]
CR0[1]	Fraction Word F1 [DB]
CR0[0]	Fraction Word F0 [DB]

SUGGESTED POWER UP SEQUENCE

INITIAL REGISTER WRITE SEQUENCE

After applying power to the part, the following register write sequence should be adhered to. Please note that CR33, 32 and 31 are readback only registers. Also note that all writeable registers should be written to on power up. Please refer to the register map for more details on all registers.

W CR30 00h: Set attenuator to 0dB gain.

W CR29 00h: Modulator is powered down. The modulator is powered down by default to ensure that no spurious signals occur on the RF output when the PLL is carrying out it's first acquisition. To avoid spurious signals, the modulator should be powered up only when the PLL is locked.

W CR28 01h: The default setting is 01h. When using an external VCO with the internal PLL synthesizer, the internal VCO needs to be powered down. This is acheived by setting CR28[5] = 1 and thus CR28 = 21h.

W CR27 00h: Power down the LO monitor. When using an external VCO or LO (whether the internal PLL synthesizer is used or not), this signal needs to be muxed through to the modulator by programming CR27[4:3] to be 01h thus making CR27 = 08h.

W CR26 00h: Reserved register.

W CR25 32h: Reserved register.

W CR24 18h: Reserved register.

W CR23 74h: Enable lock detector.

W CR22 00h: Reserved register.

W CR21 00h: Reserved register.

W CR20 00h: Reserved register.

W CR19 00h: Reserved register.

W CR18 00h: Reserved register.

W CR17 00h: Reserved register.

W CR16 00h: Reserved register.

W CR15 00h: Reserved register.

W CR14 1Bh: Attenuator is always enabled, other referenced blocks always disabled when TxDis is asserted.

W CR13 18h: Reserved register.

W CR12 08h: PLL powered up. When using an external LO without the internal PLL circuitry, the internal PLL needs to be powered down. This is achieved by setting CR12[2] = 1 and thus CR12 = 0Ch.

W CR11 00h: Reserved register.

W CR10 21h: Reference path doubler enabled and R/2 divider bypassed.

W CR9 70h: With the recommended loop filter component values and Rset = 4k7 as outlined in Fig. 8, the charge pump current is set to 2.5mA for a loop bandwidth of 80 kHz.

W CR8 00h: Reserved Register.

W CR7 0xh: Set according to equation 1 below.

The LO frequency is governed by the following equation:

$$LO = FPFD \times (INT + (FRAC/2^{25})) \quad \text{(Eq. 1)}$$

Where:

LO is the PLL output frequency.

FPFD is the PFD input frequency.

INT is the divide ratio of the binary 12-bit counter controlled by CR7 and CR6 (31 to 4095).

FRAC is the 25-bit numerator of the fractional division controlled by CR3, CR2, CR1 and CR0 (0 to $2^{25} - 1$).

W CR6 xxh: Set according to equation 1.

W CR5 00h: Disable the 5-bit reference divider.

W CR4 01h: Reserved register.

W CR3 0xh: Set according to equation 1.

W CR2 xxh: Set according to equation 1.

W CR1 xxh: Set according to equation 1.

W CR0 xxh: Set according to equation 1.

CR0 needs to be the last register written to in order for all the double-buffered bit writes to take effect.

Monitor LDET output or wait 1ms to ensure PLL is locked.

W CR29 01h: Power up modulator.

The write to CR29 does not need to be followed by a write to CR0 as it is not double-buffered.

EXAMPLE: Changing the LO Frequency

After the initialization sequence, the following is an example of how to change the LO frequency. Assume that the PLL is locked to 1.2 GHz. In this case, the following conditions apply:

FPFD = 20 MHz (assumed)

The divide ratio N = 60 so:

INT = 60 decimal so CR7 = 00h and CR6 = 3Ch.

FRAC = 0 so CR3 = 00h, CR2 = 00h, CR1 = 00h and CR0 = 00h.

Now assume the new frequency is 1.230 GHz. In the case the new registers values would be:

The divide ratio N = 61.5 so:

INT = 61 decimal so CR7 = 00h and CR6 = 3Dh.

FRAC = 16777216 so CR3 = 01h, CR2 = 00h, CR1 = 00h and CR0 = 00h.

Note CR0 should be the last write in this sequence.

APPLICATIONS SOLUTION

GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADRF6750 using the integrated VCO. It contains the following:

- the ADRF6750 IQ modulator with integrated Fractional-N PLL and VCO
- SPI and I²C interface connectors
- dc biasing and filter circuitry for the baseband inputs
- low pass loop filter circuitry
- a 10 MHz reference clock
- the ability to monitor the LOMON outputs
- SMA connectors for power supplies and the RF output

The board comes with associated software to allow easy programming of the ADRF6750.

HARDWARE DESCRIPTION

The circuit diagram is shown in Figure 11. References to it are made in the following description.

Power Supplies

An external +5V supply (DUT +5V) drives both an on-chip +3.3V regulator as well as the quadrature modulator. A breakdown of these +5V supply pins is as follows:

- VCC1 – This is the +5V regulator supply.
- VCC2 – This is the modulator output stage supply.
- VCC3 – This is the LO buffers and quadrature divider supply.
- VCC4 – This is the baseband supply.

The regulator feeds the various VREG pins on the chip with +3.3V. These VREG pins drive the following circuitry:

- VREG1 - This is the charge pump and PFD supply.
- VREG2 – This is the N-counter and bias circuit supply.
- VREG3 - This is the N-counter output supply.
- VREG4 – This is the reference clock, lock detect and autocal supply.
- VREG5 – This is a digital supply for the serial port and sigma-delta modulator.
- VREG6 – This is the VCO supply.

The external reference clock generator can be driven by a +3.3V supply. This supply can be connected via an SMA connector VCO +V.

Recommended Decoupling for Supplies

The external +5V supply is decoupled initially by a 10uF capacitor and then further by a parallel combination of 100nF and 10pF capacitors which are placed as close to the DUT as possible for good local decoupling. The regulator output should ideally see between 300nF and 3uF capacitance. The schematic shows a parallel combination of 470nF and 10pF on the regulator output and then a parallel combination of 100nF and 10pF on each VREG pin. Again these capacitors are placed as close to the pins as possible. The total capacitance that the regulator sees excluding parasitics is then roughly 1.1uF. The impedance of all these capacitors should be low and constant across a broad frequency range. Surface mount multi-layered ceramic chip (MLCC) class II capacitors provide very low ESL and ESR which assist in decoupling supply noise effectively. They also provide good temperature stability and good ageing characteristics. Capacitance also changes versus applied bias voltage. Larger case sizes have less capacitance change versus applied bias voltage and also have lower ESR but higher ESL. 0603 size capacitors provide a good compromise. X5R and X7R capacitors are examples of these types of capacitors and are recommended for decoupling.

SPI and I2C Interface

The SPI interface connector is a 9-way D-type connector which can be connected to the printer port of a P.C. The PC cable diagram which is required to be used with the provided software is shown in Figure 10 below.

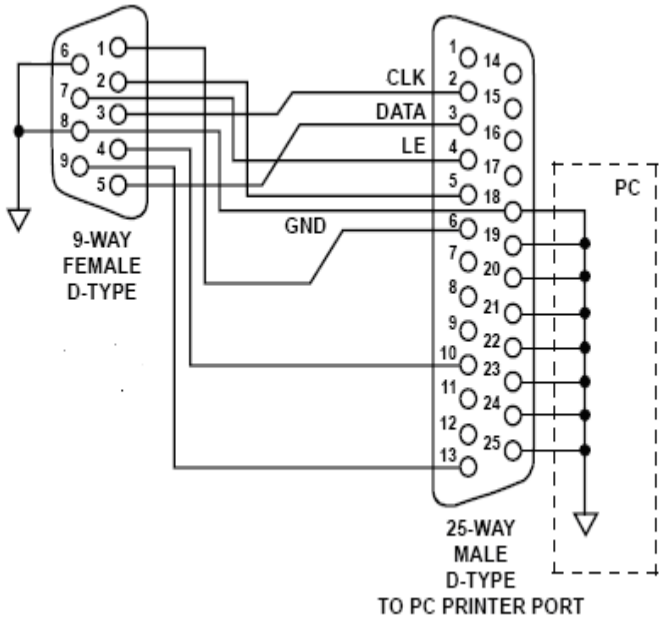

Figure 10. SPI PC Cable Diagram

There is also an option to use the I²C interface by using the I²C receptacle connector. This is a standard I²C connector. +5V power is provided by the I²C bus master. Pull-up resistors are required on the signal lines. CS can be used to set the slave address of the AD45110. CS high sets the slave address to 60H and CS low sets the slave address to 40H.

Baseband Inputs

The pair of I and Q baseband inputs are served by SMA inputs so that they can be driven directly from an external generator which may also provide the dc bias required. An option is provided to supply this de bias through connector J1 as well. The option to filter the baseband inputs is also provided although these may not be required depending on the quality of the baseband source.

Loop Filter

A 4th order loop filter is provided at the output of the charge pump. With the charge pump current set to a mid-scale value of 2.5mA and using the on-chip VCO, the loop bandwidth is approximately 80 kHz and the phase margin 55°. COG capacitors are recommended for use in the loop filter as they have low dielectric absorption which is required for fast and accurate settling time. The use of non-COG capacitors may result in a long tail being introduced into the settling time transient.

Reference Input

The reference input can be supplied by a 10 MHz clock generator or by an external clock through the use of J7. The frequency range of the reference input is from 10MHz to 20MHz and thus if the lower frequency is used, the on-chip reference doubler should be employed to set the PFD frequency to 20MHz in order to optimise phase noise performance.

LOMON Outputs

These are differential LO monitor outputs which provide a replica of the internal LO frequency at 1xLO. The single-ended power in a 50Ω load can be programmed to either -24dBm, -18dBm, -12dBm or -6dBm. The outputs are open-collector outputs which need to be terminated to +3.3V. As both outputs need to be terminated to 50Ω, options are provided to terminate to +3.3V by on-board 50Ω resistors or by series inductors (or a ferrite bead) in which case the 50Ω, termination would be provided by the measuring instrument. If not used, these outputs should be grounded.

CCOMP Pins

These are internal compensation nodes which need to be decoupled to ground with a 100nF capacitor.

MUXOUT

This is a test output which allows different internal nodes to be monitored. It is a CMOS output stage which can be driven un-terminated.

LDET

Lock detect is a CMOS output which indicates the state of the PLL, a high level indicates a locked condition while a low level indicates a loss of lock condition.

TXDIS

This input disables the RF output. It can be driven from an external stimulus or just connected high or low by jumper J18.

RF Output

RFOUT is the RF output of the ADRF6750.

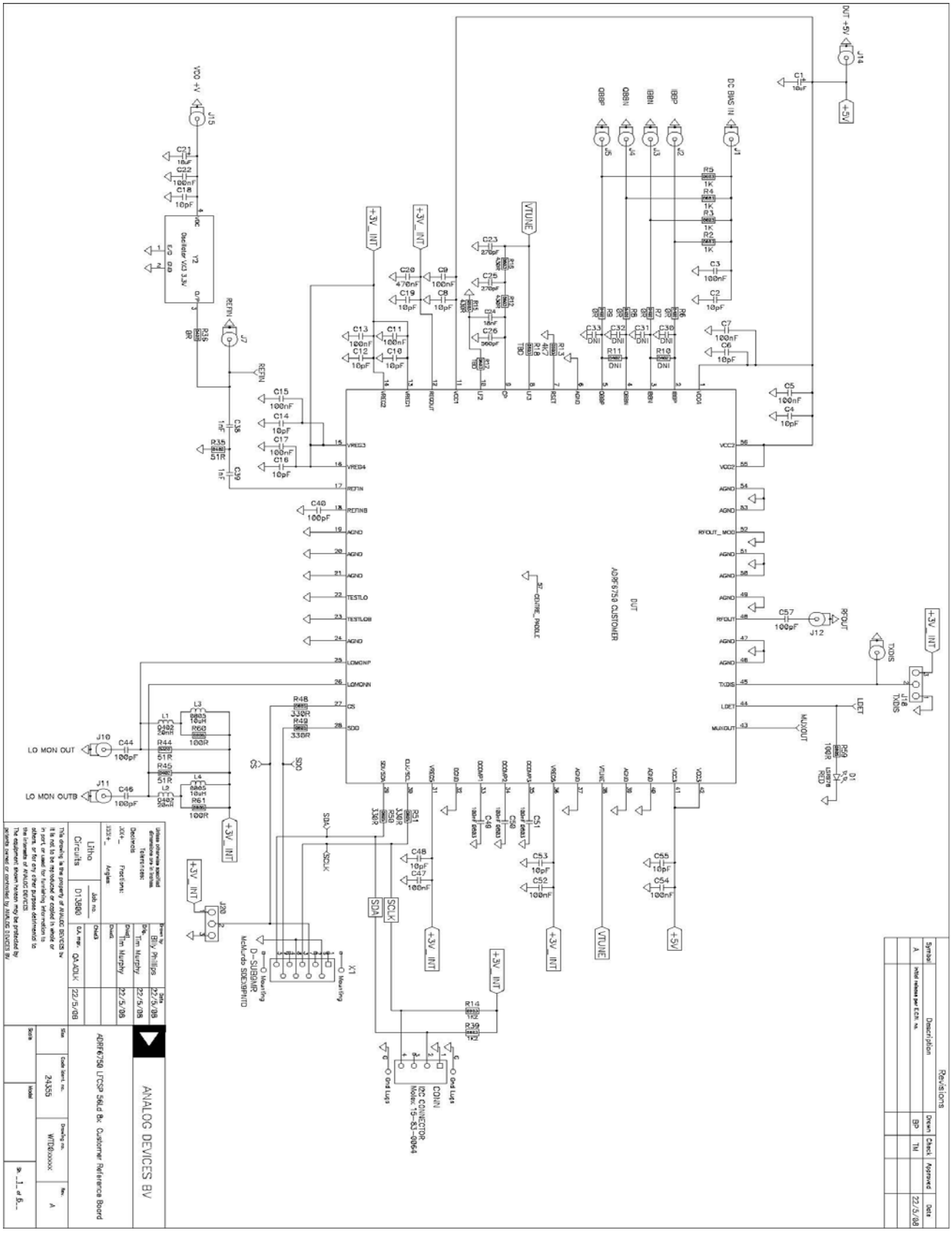

Figure 11. ADL5594 Applications Circuit

BILL OF MATERIALS

Table 4: Bill Of Materials

Name	Part Type	Value	Description	Part Number
DUT	LFCSP IC		ADRF6750 LFCSP 56Lead 8X8 0.50mm	ADI Supplied
Y2	TCVCXO	10MHz	VCO 10MHz Jauch	10.0-VX3MQ-LF
CONN1	Connector	D-SUB9MR	Connector, 9 Pin D-Sub Plug	FEC 150-750
CONN2	Connector	Molex Conn	Connector Molex Semconn Receptacle	15-83-0064
C1	CAP	10uF	25V Tantelum TAJ-C	FEC 197-518
C2	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C3	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C4	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C5	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C6	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C7	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C8	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C9	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C10	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C11	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C12	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C13	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C14	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C15	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C16	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C17	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C18	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C19	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C20	CAP	470nF	16V Y5V Ceramic 0603	FEC 318-8851
C21	CAP	10uF	25V Tantelum TAJ-C	FEC 197-518
C22	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C23	CAP	270pF	50V COG Ceramic 0603 Murata	FEC 140-3568
C24	CAP	18nF	50V COG Ceramic 1206 Murata	FEC 882-0171
C25	CAP	270pF	50V COG Ceramic 0603 Murata	FEC 140-3568
C26	CAP	560pF	50V COG Ceramic 0603 Murata	FEC 140-3585
C38	CAP	1nF	50V COG Ceramic 0402 Murata	FEC 881-9556
C39	CAP	1nF	50V COG Ceramic 0402 Murata	FEC 881-9556
C40	CAP	100pF	50V COG Ceramic 0402 Murata	FEC 881-9572
C44	CAP	100pF	50V COG Ceramic 0402 Murata	FEC 881-9572
C46	CAP	100pF	50V COG Ceramic 0402 Murata	FEC 881-9572
C47	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C48	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C49	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C50	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C51	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C52	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C53	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C54	CAP	100nF	25V X7R Ceramic 0603	FEC 317-287
C55	CAP	10pF	50V COG Ceramic 0402 Murata	FEC 881-9564
C57	CAP	100pF	50V COG Ceramic 0402 Murata	FEC 881-9572
J18	Jumper		Jumper 3 Pin + Shunt	FEC 148-533 + FEC 150-411
J20	Jumper		Jumper 3 Pin + Shunt	FEC 148-533 + FEC 150-411

L1	IND	20nH	0402 Murata LQW Series	LQW15AN20N
L2	IND	20nH	0402 Murata LQW Series	LQW15AN20N
L3	IND	10uH	0805 Murata LQM Series	LQM21FN1N100M
L4	IND	10uH	0805 Murata LQM Series	LQM21FN1N100M
D1	Diode	LSR976	Diode Sm LED RED HYPER-BRIGHT 20mA 0805	FEC 122-6392
R2	RES	1K	1/10W 5% 0603 Bourns	CR0603-JW-102
R3	RES	1K	1/10W 5% 0603 Bourns	CR0603-JW-102
R4	RES	1K	1/10W 5% 0603 Bourns	CR0603-JW-102
R5	RES	1K	1/10W 5% 0603 Bourns	CR0603-JW-102
R6	RES	0R	1/16W 1% 0402	FEC 115-8241
R7	RES	0R	1/16W 1% 0402	FEC 115-8241
R8	RES	0R	1/16W 1% 0402	FEC 115-8241
R9	RES	0R	1/16W 1% 0402	FEC 115-8241
R10	RES	DNI	Resistor Spacing 0402	TBD
R11	RES	DNI	Resistor Spacing 0402	TBD
R12	RES	430R	1/10W 0.1% 0603	FEC 140-0557
R13	RES	4K7	1/10W 1% 0603	CR0603-FX-472
R14	RES	1K2	1/16W 1% 0603	FEC 923-3393
R15	RES	430R	1/10W 0.1% 0603	FEC 140-0557
R16	RES	430R	1/10W 0.1% 0603	FEC 140-0557
R17	RES	DNI	Resistor Spacing 0603	TBD
R18	RES	DNI	Resistor Spacing 0603	TBD
R35	RES	51R	1/16W 5% 0402 Bourns	CR0402-JW-510
R36	RES	0R	1/16W 1% 0402	FEC 115-8241
R39	RES	1K2	1/16W 1% 0603	FEC 923-3393
R44	RES	51R	1/16W 5% 0402 Bourns	CR0402-JW-510
R45	RES	51R	1/16W 5% 0402 Bourns	CR0402-JW-510
R48	RES	330R	1/10W 5% 0805 Bourns	CR0805-JW-331
R49	RES	330R	1/10W 5% 0805 Bourns	CR0805-JW-331
R50	RES	330R	1/10W 5% 0805 Bourns	CR0805-JW-331
R51	RES	330R	1/10W 5% 0805 Bourns	CR0805-JW-331
R59	RES	100R	1/10W 5% 0805	CR0805-JW-101
R60	RES	100R	1/10W 5% 0805	CR0805-JW-101
R61	RES	100R	1/10W 5% 0805	CR0805-JW-101
J1	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J2	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J3	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J4	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J5	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J7	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J7	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J10	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J11	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J12	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J14	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J15	SMA		SMA Side Launch Connector	Johnson 142-0701-851
J15	SMA		SMA Side Launch Connector	Johnson 142-0701-851
CS	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	
LDET	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	
MUXOUT	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	
REFIN	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	
SCLK	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	

SDA	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	
SDO	TESTPOINT		TEST POINT ONE PIN 0.35in Dia	

OUTLINE DIMENSIONS

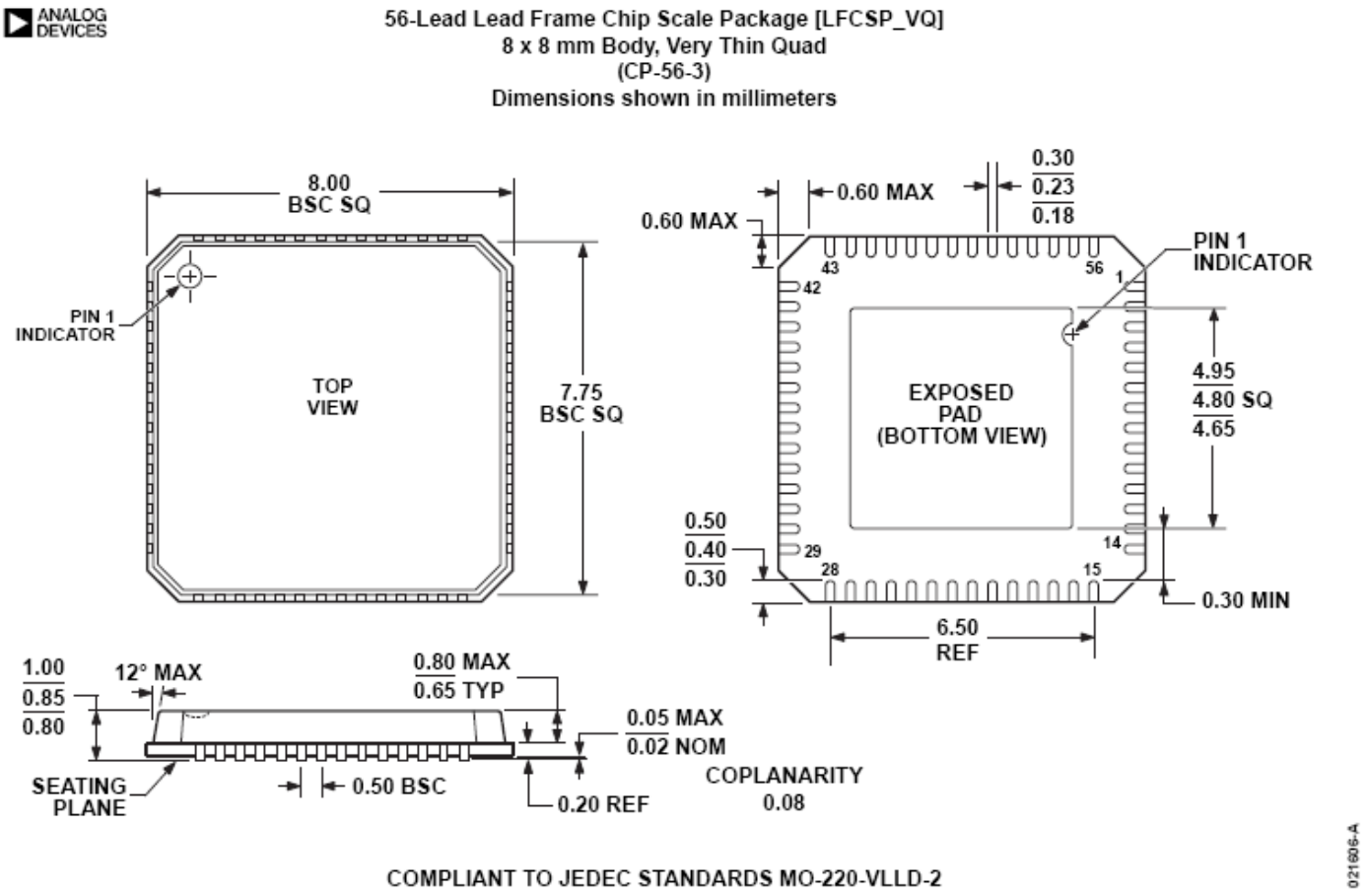

Figure 12. 56-Lead LFCSP with exposed paddle. Dimensions shown in millimeters

TABLE 38. ORDERING GUIDE

Model	Temperature Range (°C)	Package Description	Package Option
ADRF6750ACPZ[1]	0 to +70	Tray	LFCSP

[1] Z indicates Pb-free